

0 multiplexer circuitry, coupled to the output driver
11 circuitry, to provide the first and second portions of data to the
12 output driver circuitry.

1 ¹⁷~~167~~. (Amended) The memory controller of claim ¹⁶~~166~~ [further
2 including: multiplexer circuitry coupled to the output driver
3 circuitry,] wherein:

4 in response to the rising edge [first] transition of
5 the external clock signal, the multiplexer circuitry
6 provides [couples the first portion of] data to [an input
7 of] the output driver circuitry; and

8 in response to the falling edge [second] transition of
9 the external clock signal, the multiplexer circuitry
10 provides [couples the second portion of] data to [the input
11 of] the output driver circuitry.

[In claim 168, line 5, delete "the input of".

] In claim 169, line 4, delete "input of the".

1 ²²~~172~~. (Amended) A memory controller for controlling a synchronous
2 memory device, the memory controller comprising:

3 output driver circuitry to output data wherein:

4 the output driver circuitry outputs a first portion of
5 data in response to a first external clock signal; and

6 the output driver circuitry outputs a second portion of
7 data in response to a second external clock signal; and

8 multiplexer circuitry coupled to the output driver
9 circuitry, to provide the first and second portions of data to the
10 output driver circuitry.

1 ²³
173. (Amended) The memory controller of claim ²²
2 ~~172~~, further
including:

3 multiplexer circuitry coupled to the output driver circuitry,]

4 wherein:

5 in response to the first external clock signal, the
6 multiplexer circuitry provides [couples the first portion of] data
7 to [an input of] the output driver circuitry; and

8 in response to the second external clock signal, the
9 multiplexer circuitry provides [couples the second portion of]
10 data to [the input of] the output driver circuitry.

[In claim 174, line 5, delete "the input of".

[In claim 175, line 4, delete "input of the".